Memory Ordering Instructions in Intel x86_64 and ARMv8-A

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June 29, 2026

1 Overview

This document provides a compact, semi-formal summary and comparison of explicit memory ordering instructions in Intel's x86_64 and ARMv8-A+ architectures, relevant to inter-thread synchronization, timing, and IO. It builds on knowledge of the core x86 and ARM memory ordering models. I recommend this blog post for an overview, and the Intel / ARM manuals referenced in the sources section for a more detailed and formal treatment.

2 X86_64

Load instructions are considered globally visible once the value that will be loaded into the destination register is determined. The memory access has been completed, but the destination register isn't necessarily filled.

Store instructions are considered globally visible at the point in time where the value written by the store might be read by any other logical processor.

Store instructions are considered locally complete when their values have been committed to memory / cache subsystem, but they may not be entirely propagated throughout it yet. This is a weaker condition than globally visible.

2.1 SFENCE

Waits for all previous stores to become globally visible before SFENCE completes, and before any store after SFENCE becomes globally visible. Ordered with respect to stores, SFENCE, MFENCE, and any serializing instructions. Not ordered with respect to loads or LFENCE.

For temporal stores to write back (WB) memory, there is a single order of global visibility consistent w.r.t. program order on all logical processors (e.g. if a core writes to A then B, all other cores will observe writes to A then B), so there is no benefit to using SFENCE. For stores to write combining (WC) memory and non-temporal stores to WB, stores may not appear in program order (e.g. if a core writes A then B, others may observe changes to B then A), and thus an SFENCE should be used to enforce a consistent global ordering.

2.2 LFENCE

Waits for all prior instructions to complete locally and receive memory, and no later instruction executes until LFENCE is completed (not even speculatively, although they may be fetched and decoded). Blocking execution makes LFENCE useful for speculation hardening, but makes it slightly worse for measuring very short timescales (e.g. differentiating L1/L2 accesses), as it introduces longer and noisier latencies for instructions immediately following the LFENCE. Note LFENCE's pre-condition - it guarantees that prior instructions have been completed, not that they are globally visible.

Loads always appear to execute in a globally consistent program order, except in the case of intra-processor forwarding, where a processor may load from it's own store buffer before that store is visible to other logical processors.

2.3 MFENCE

Waits for all prior loads and stores to be globally visible before executing and before all following loads/stores. Ordered with respect to all loads and stores, MFENCE, LFENCE, SFENCE, and serializing instructions, although it does not serialize the whole instruction stream.

2.4 RDTSCP (Not a memory ordering inst, but useful for timing)

Waits for all prior instructions to have been executed and for all prior loads to be globally visible. RDTSC is similar, but does not provide any such guarantee. According to the Intel Software Developer Manual, if you want RDTSCP to only be run after previous stores are completed, add an MFENCE before it, and if you want RDTSCP to be executed before any subsequent instruction, add an LFENCE after it.

3 ARMv8-A

From the ARMv8-A architecture manual:

- A read/write RW1 is observed by a write W2 from iff W2 is coherence-after RW1.
- A write W1 is observed by a read R2 iff R2 reads from W1.
- A read R2 reads from a write W1 to the same location iff R2 takes its data from W1.

3.1 Data Memory Barrier (DMB)

All memory accesses and cache maintenance operations of the relevant type are ordered before and after the DMB operation. This means that all prior relevant memory accesses are observed by all relevant memory accesses after the DMB operation. It does not guarantee the completion of any memory accesses.

3.2 Data Synchronization Barrier / Data Write Barrier (DSB)

All prior memory accesses (of the relevant type), cache maintenance, and TLB operations are completed before the DSB is completed. No instructions after the DSB may execute except for being fetched and decoded, and reading registers that don't cause side effects (very limited).

3.3 Relevant Type (for both DSB and DMB)

- **SY / OSH / ISH:** Waits for prior stores and loads, and constrains loads and stores after the instruction. This is the default.
- **ST / OSHST / ISHST:** Waits for prior stores, and constrains stores after the instruction.
- **LD / OSHLD / ISHLD:** Waits for prior loads, and constrains loads and stores after the instruction. Only available on ARMv8+.

3.4 Sharability Domain (for both DSB and DMB)

- **Full System:** SY, ST, and LD referring to all memory devices. Slowest.
- **Outer Sharability Domain:** OSH, OSHST, and OSHLD wait for and constrain instructions in a set of inner sharability domains. Used for non-coherent DMA. Faster than full system.
- **Inner Sharability Domain:** ISH, ISHST, and ISHLD only wait for and constrain instructions in all devices coherent with the memory location. This is useful for DMA and MMIO, and is the fastest.

4 Comparison

	Restricts prior			Restricts future		
Instruction	Loads	Stores	Other	Loads	Stores	Other
MFENCE	Y (G)	Y (G)	N	Y	Y	N
LFENCE	Y (L)	Y (L)	Y (L)	Y	Y	Y
SFENCE	N	Y (G)	N	N	Y	N
DSB SY	Y	Y	N	Y	Y	Y
DSB ST	N	Y	N	Y	Y	Y
DSB LD	Y	N	N	Y	Y	Y
DMB SY	Y	Y	N	Y	Y	N
DMB ST	N	Y	N	N	Y	N
DMB LD	Y	N	N	Y	Y	N

5 Notes

- For x86_64, by default the restrictions mean that future instructions will become globally visible after the prior instructions become globally visible, not necessarily completed or executed. Note that LFENCE provides a different guarantee.
- For DMB, the restriction means that prior instructions are observed by future instructions, not necessarily completed or executed.
- For DSB, the restriction means that prior memory operations are guaranteed to be completed before any future instruction executes.
- This table only holds for ARMv8-A. ARMv8-R relaxes some DMB restrictions, and previous ISA revisions describe a stricter DMB ST.
- LFENCE guarantees all prior instructions' local completion. MFENCE restricts only prior loads and stores, but ensures global visibility.

6 Rough ARM Analogues for x86 Operations

- MFENCE is most similar to DMB SY to enforce memory ordering, although DSB SY may be safer for timing-critical operations or speculation hardening as it blocks execution.
- SFENCE is most similar to DMB ST to enforce memory ordering, although DSB ST may be safer for timing-critical operations or speculation hardening as it blocks execution.
- LFENCE is most similar to DSB SY, but LFENCE restricts all prior instructions, not just memory ones.

7 Sources

- Intel® 64 and IA-32 Architectures Software Developer's Manual
- Intel® 64 and IA-32 Architectures Optimization Reference Manual
- ARM® Architecture Reference Manual - ARMv8, for ARMv8-A architecture profile
- ARM Memory Barriers Documentation